FEATURES

- 2 layer feed forward analog artificial neural network
- 200 weight cells (synapses)
- 20 bias weight cells
- 10 inputs
- 10 outputs
- 10 hidden neurons
- fast response time (<1 µs)
- 10bit DAC and 10bit ADC

APPLICATIONS

- fast classification tasks
- control systems
- sensor signal processing
- sensor signal adaptation

FUNCTIONALITY

The functionality of a neural network can be described as consecutive (as many as network layers) vector-matrix dot multiplications. Assuming two network layers, the process is as follows. The signals applied to the chip inputs form the input vector (in). This vector is dot multiplied by the first matrix of weight values (w1). The result is a vector that is again dot multiplied by the second matrix of weight values (w2) delivering the output vector (out). The following equation gives an example using a 3-4-2 network topology, i.e. 3 inputs, 4 hidden neurons and 2 outputs.The procedure, the proper weight values are determined is called the adaptive process (training).

$$\begin{bmatrix} out_1 \\ out_2 \end{bmatrix} = \left[\begin{bmatrix} in_1 \\ in_2 \\ in_3 \end{bmatrix}^T \cdot \begin{bmatrix} w1_{1,1} & w1_{2,1} & w1_{3,1} \\ w1_{1,2} & w1_{2,2} & w1_{3,2} \\ w1_{1,3} & w1_{2,3} & w1_{3,3} \\ w1_{1,4} & w1_{2,4} & w1_{3,4} \end{bmatrix}^T \right] \cdot \ldots$$

$$\ldots \begin{bmatrix} w2_{1,1} & w2_{1,2} & w2_{1,3} & w2_{1,4} \\ w2_{2,1} & w2_{2,2} & w2_{2,3} & w2_{2,4} \end{bmatrix}^T$$

DESCRIPTION

The **Silimann® 220ADDA** is a VLSI integrated artificial neural network chip performing any function trainable with the given network topology. The training is done by a host computer and special training software. The neural network part of the device is fully parallel and analog. It contains a 10-10-10 network topology (i.e. 10 inputs, 10 hidden neurons and 10 outputs). 200 regular synapses are employed. Additionally there are 10 bias synapses in the hidden layer and 10 bias synapses in the output layer. These bias synapses are supplied with a constant signal. In total, the network holds 220 synapses.

The **Silimann® 220ADDA** is controlled by a digital modul with serial interface to configure the chip, to address the synaptic weights and to controll DAC and ADC.
Since the weight storage is realized capacitively, a cyclic refresh of the weight values must be implemented externally.

ABSOLUTE MAXIMUM RATINGS

- positive digital supply voltage (VDD) : 5.5 V
- negative digital supply voltage (GND) : 0 V
- positive analog supply voltage (VDDA) : 5.5 V
- negative analog supply voltage (VSSA) : 0 V
- input signal voltages must not exceed supply voltage
- output termination resistor : ≤2 kΩ

OPERATING CONDITIONS

- ambient temperature : wide temperature range*[1]
- digital supply voltage (VDD) : 5 V (±1%)
- analog supply voltage (VDDA) : 5 V (±1%)
- analog supply voltage (AGND) : 2.2 V (±1%)
- supply current : 100 µA (±1%)
- bias value : VDDA
- output termination resistor : ≤2 k

[1] due to the training procedure, temperature effects can almost arbitrarily be balanced out

TERMINAL SPECIFICATIONS

1	VDDA<0>	supply voltage	5V	analog
2	IN<0>	signal input/output	1.2V-3.2V	analog
3	IN<1>	signal input/output	1.2V-3.2V	analog
4	IN<2>	signal input/output	1.2V-3.2V	analog
5	IN<3>	signal input/output	1.2V-3.2V	analog
6	IN<4>	signal input/output	1.2V-3.2V	analog
7	IN<5>	signal input/output	1.2V-3.2V	analog
8	IN<6>	signal input/output	1.2V-3.2V	analog
9	IN<7>	signal input/output	1.2V-3.2V	analog
10	IN<8>	signal input/output	1.2V-3.2V	analog
11	IN<9>	signal input/output	1.2V-3.2V	analog
12	VSSA<2>	ground	0V	analog
13	ON<0>	signal input/output	1.2V-3.2V/-500…+500µA	analog
14	ON<1>	signal input/output1	.2V-3.2V/-500…+500µA	analog
15	ON<2>	signal input/output	1.2V-3.2V/-500…+500µA	analog
16	ON<3>	signal input/output	1.2V-3.2V/-500…+500µA	analog
17	ON<4>	signal input/output	1.2V-3.2V/-500…+500µA	analog
18	ON<5>	signal input/output	1.2V-3.2V/-500…+500µA	analog
19	ON<6>	signal input/output	1.2V-3.2V/-500…+500µA	analog
20	ON<7>	signal input/output	1.2V-3.2V/-500…+500µA	analog
21	ON<8>	signal input/output	1.2V-3.2V/-500…+500µA	analog
22	ON<9>	signal input/output	1.2V-3.2V/-500…+500µA	analog
23	VDDA<1>	supply voltage	5V	analog
24	VSSA<1>	analog ground	0V	analog
ana5	VrefN	voltage reference (please connect R_{vrefN}= 10kOhm)	1.2V	analog
26	VrefP	voltage reference (please connect R_{vrefP}= 10kOhm)	3.2V	analog
27	Iref	current reference(please connect R_{iref}= 12.1kOhm)	100uA	analog
28	AGND	voltage supply	2.2V	analog
29	VDD_core2	voltage supply (core2)	5V	digital
30	VSS_core2	ground (core2)	0V	digital
31	clk	interface (clock)	0V or 5V	digital
32	rst	interface (reset)	0V or 5V	digital
33	set	interface (set)	0V or 5V	digital
34	shift	interface (shift)	0V or 5V	digital
35	write	interface (write)	0V or 5V	digital
36	in	interface (input)	0V or 5V	digital
37	out	interface (output)	0V or 5V	digital
38	VSS_peri	ground (pads)	0V	digital
39	VDD_peri	supply	5V	digital
40	VDD_core1	voltage supply (core1)	5V	digital
41	VSS_core1	ground (core1)	0V	digital
42	ADC	signal input/output	1.2V-3.2V	analog
43	AS_in	signal input/output	1.2V-3.2V	analog
44	VSSA<0>	ground	0V	analog

Table 1: Terminal Specifications

BLOCK DIAGRAM

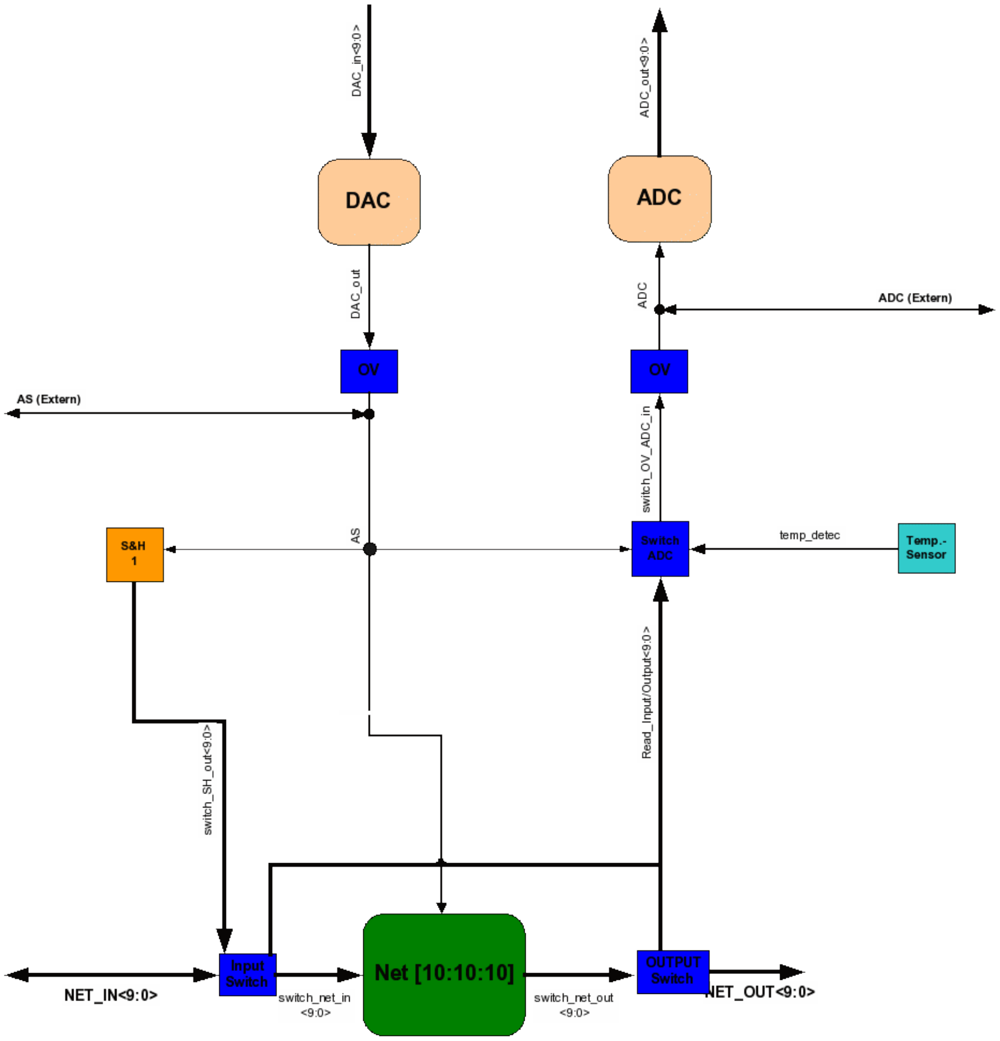


Illustration 1: Block Diagram

NET TOPOLOGIE

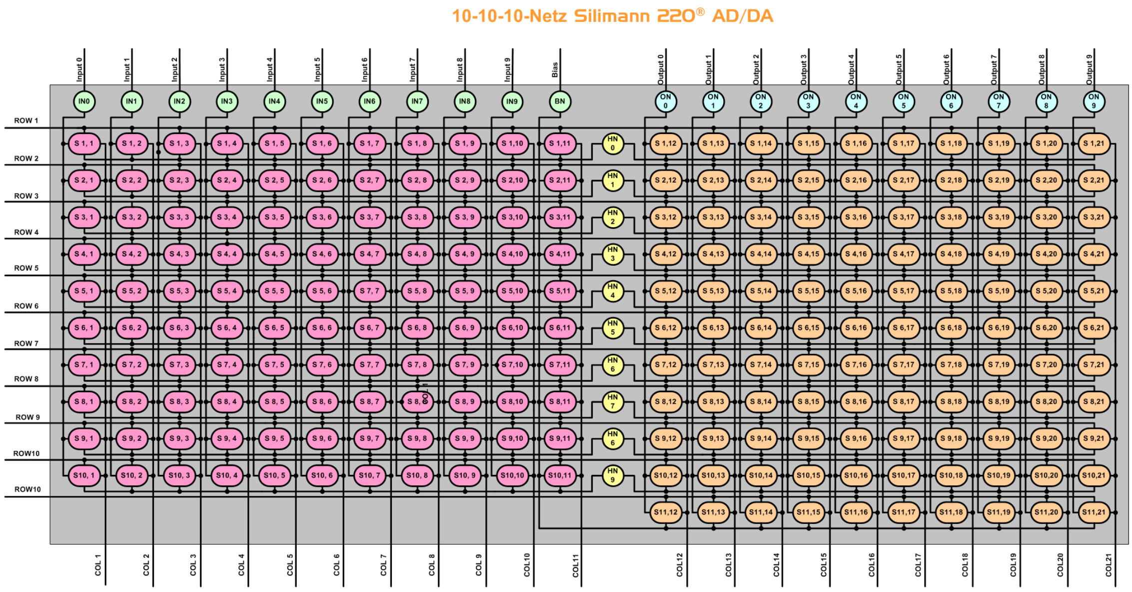


Illustration 2: Net Topologie

DIGITAL INTERFACE

The serial interface consists of 7 signal pins.

The synapses are arranged in 11 rows and 21 columns.

SIGNAL DESCRIPTION

Signal	Direction	Function
clk	I	clock (modul works on a rising edge of a clock)
rst	I	reset (low-activ)
set	I	process code (from serial buffer)
shift	I	enable shift from input
in	I	input to serial buffer
out	O	output from serial buffer
write	I	write enable (to refresh synapses)

Table 2: DIGITAL INTERFACE

The serial interface reads per clock data from **in** and shift this into the 22 bit serial buffer. (If simply **shift** is high and **reset** is not activ (high) while **clock** is connected, the signal change from **input** can be read from **out** 22 clocks later.)

The first 12 bits of the serial buffer (addr[0:1];D[0:9]) can be processed if **set** is high.
Four types of pattern can be processed:

command – configure and control
DAC-input – input a 10-bit value to be converted
row/column – input an adress
out-mux – choose data to output

and code is shown in table:

Function	addr [0:1]	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9
command	00	K0	K1	K2	K3	see below					
DAC-input	10	DAC-input (10bit)									
row/column	01	C0	C1	C2	C3	C4	R0	R1	R2	R3	X
out-mux	11	O0	O1	O2	O3	X	X	X	X	X	X

Table 3: addr [0:1]

K[0:3]	D4	D5	D6	D7	D8	D9	Description
0000	X	X	X	X	X	X	No Operation
1000	X	X	X	X	X	X	Soft-Reset
0100	X	X	X	X	X	X	ADC-Conversion
1100	CF0	CF1	CF2	CF3	X	X	**CF[3:0]**
0010	SI0	SI1	SI2	SI3	X	X	Switch-In **SI[3:0]**
1010	X	SO0	SO1	SO2	X	X	Switch-Out **SO[2:0]**
1110	Aa0	Aa1	X	X	X	X	Switch-ADC **Aa [1:0]**
0001	Ab0	Ab1	Ab2	Ab3	X	X	Switch-ADC **Ab [3:0]**
1001	PD0	PD1	PD2	X	X	X	Power Down **PD[2:0]**
0101	SH0	SH1	SH2	SH3	X	X	Sample-and-Hold **SH [3:0]**

Table 4: K[3:0]

CF[3:0]	function
XXX1	AS-OV off
XX1X	ADC-OV off
X1XX	ADC clock enable
1XXX	ADC-clock not inverted
X: influences the other settings from this table!	

Table 5: CF[3:0]

SI[3:0]	connect with switch SI	direction
XXX1	sample-and-hold	I
XX0X	IN-pins	I/O
X1XX	pass to ADC/SO	I/O
0XXX	net-in	O
X: influences the other settings from this table!		

Table 6: SI[3:0]

SO[2:0]	connect with switch SO	direction
XX0	net-out	I
X0X	ON-pins	I/O
1XX	ADC-switch	O
X: influences the other settings from this table!		

Table 7: SO[2:0]

Aa[1:0]	Bit	Function
01	10	Temp Sensor aufschalten Ab[3:0]=0000
10	11	AS Signal aufschalten Ab[3:0]=0000

Table 8: Aa[1:0]

Ab[3:0]	switch to ADC
0000	open
0001	<0> (from SI / SO)
0010	<1> (from SI / SO)
0011	<2> (from SI / SO)
0100	<3> (from SI / SO)
0101	<4> (from SI / SO)
0110	<5> (from SI / SO)
0111	<6> (from SI / SO)
1000	<7> (from SI / SO)
1001	<8> (from SI / SO)
1010	<9> (from SI / SO)
Do not switch more than one source to ADC: Aa[1:0]=00	

Table 9: Ab[3:0]

PD[2:0]	Function
XX1	internal references off
X1X	internal sensor (temperature) off
1XX	sample-and-hold off
X: influences the other settings from this table!	

Table 10: PD[2:0]

SH [3:0]	Bit	write to Sample-and-Hold
0000	-	initial state (after reset)
0001	0	<0>
0010	1	<1>
0011	2	<2>
0100	3	<3>
0101	4	<4>
0110	5	<5>
0111	6	<6>
1000	7	<7>
1001	8	<8>
1010	9	<9>

Table 11: SH[3:0]

O0-O3	Ausgang
0000	ADC Out (standard)
1000	DAC Wert
0100	Zeile / Spalte
1100	Konfiguration
0010	Switch In
1010	Switch Out
0110	Switch Temp
1110	Switch ADC (A)
0001	Switch ADC (B)
1001	Switch AS
0101	Switch SH
1111	Outmux

Table 12: Outmux O[0:3]

To process the command data D[9:0];addr[1:0] is shifted into **in:**

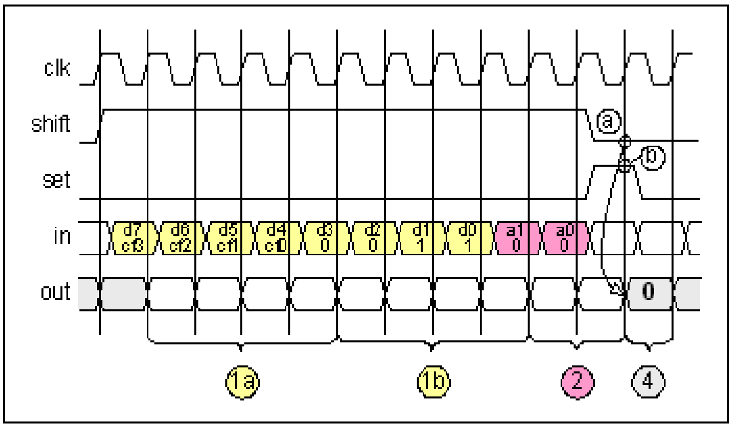


Illustration 3: To process the command data

- The 12 bits are sent, first bit is D<9> and last is addr<0>. With every rising edge of clock the data connected to **in** is shifted into the serial buffer, **shift** must be high. (1a, 1b, 2)
- After 12 clocks next rising edge of clock **shift** must be low (a). To process command **set** must be high (b).
- **out** changes to 0 for one clock, command is processed.

To read from serial buffer first the out-mux is used to select source to read from.

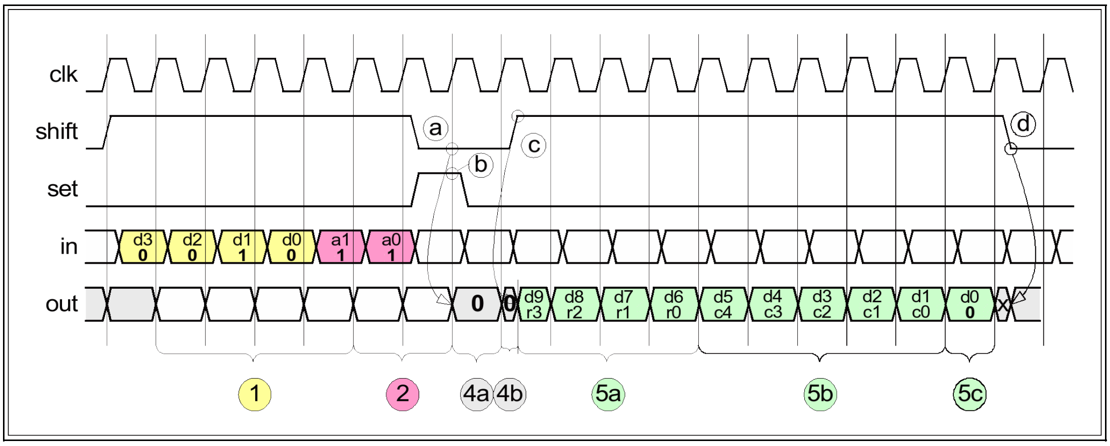


Illustration 4: To read from serial buffer

- up to (b) same as **To process the command data**
- next clock to let the out-mux switch (4a)
- with setting **shift** to high data from the selected source is written to serial buffer D[12:21]. This happens immediately (asychron to clock), i.e. **out** must be read between setting **shift** to high and next rising edge of clock!
- after next 9 rising edges of clock each time data is read from **out** (5a,5b,5c)

ADC-conversion (prior to this please enable ADC-clock)

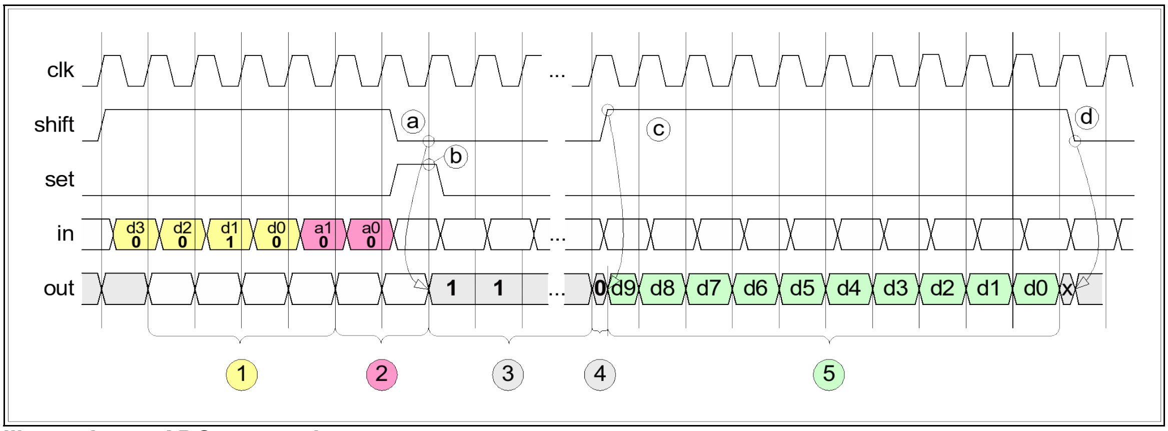


Illustration 5: ADC-conversion

- up to (b) the same as in **To process the command data (**command is xxxxxx001000)
- **out** changes to 1 here, showing ADC is still converting (busy),(3)
- 12 clocks later **out** changes to 0, ADC is ready
- from here on (4) data can read as in **To read from serial buffer**

write to synapses:

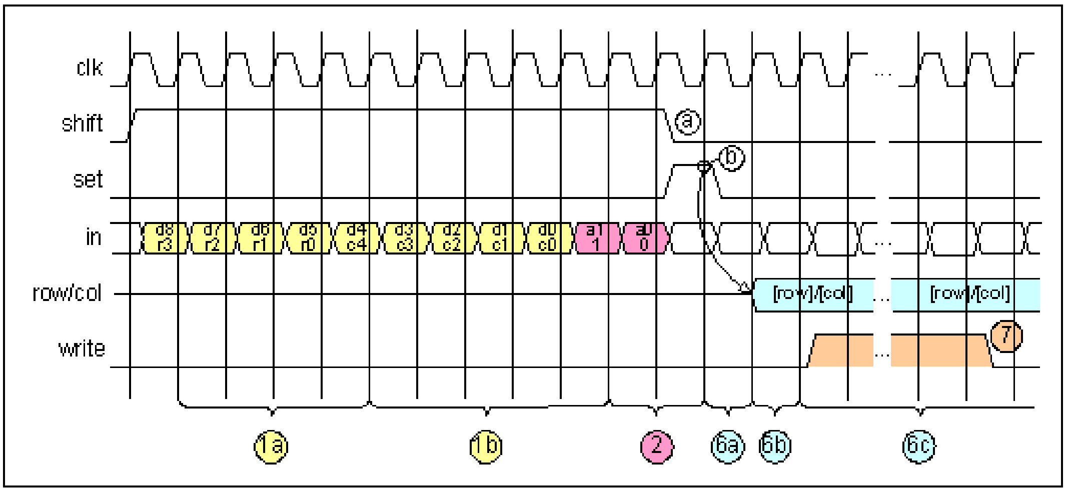


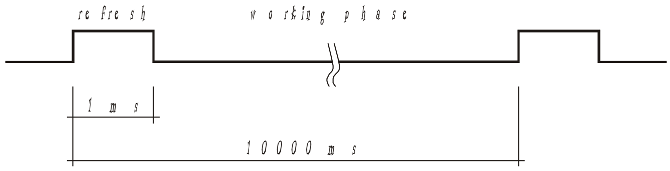
Illustration 6: write to synapses

- up to (b): send selected row/column as in **To process the command data**
- next clock (6a) to adress the selected synapse
- waiting 1µs adress settlig time (6b)
- write (asyncron) is high, voltage from AS is written to selected synapse (10µs at least)

TIMING CONCIDERATIONS

Since the synaptic values are stored capacitively, they must be refreshed at regular intervals. One refresh per 10000 ms is sufficient to garantee stable values. About 7 µs are required to address and load a single synapse. In total, a complete resfresh cycle for all synapses takes less than a millisecond. The quality of the signal processing could be slightly affected during this short transaction.

REFRESH SCHEME



PERFORMANCE CHARACTERISTICS

WEIGHT CELL DROOP RATE vs. TIME (selection)

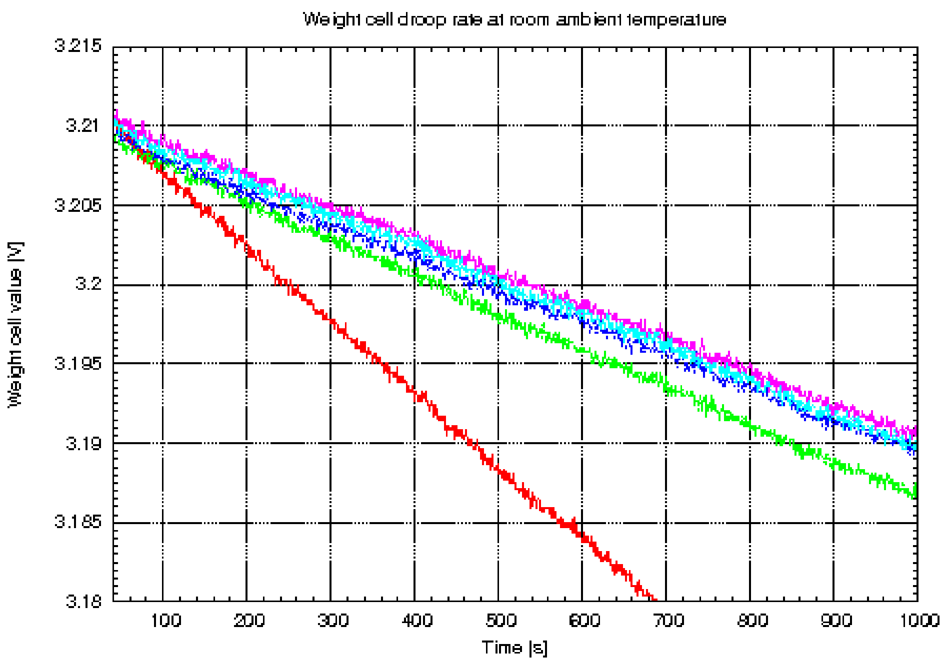


Illustration 7: Weight Cell Droop Rate

RESPONSE TIME

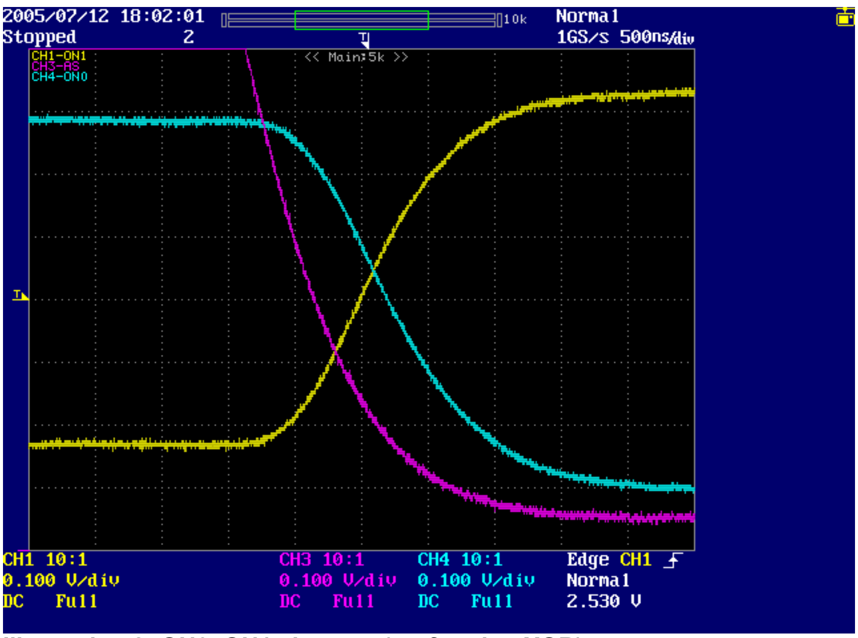
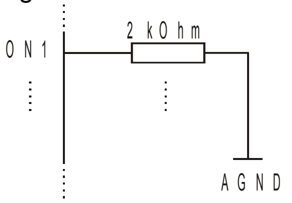


Illustration 8: ON0, ON1 changes (performing XOR)

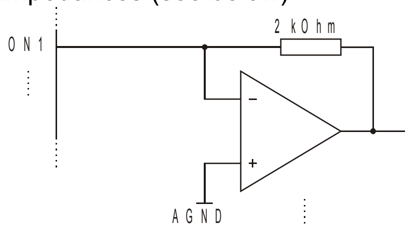
APPLICATION INFORMATION

OUTPUT TERMINATION

The net-outputs of the **Silimann® 220AD/DA** are current outputs. For proper operation, they should be terminated with 2 kOhm resistors against AGND.



By these terminators, the output current of ± 500 µA is converted into a voltage drop of ±1 V. It is recommended to do the termination actively (using Operational Amplifiers) to lower the output impedances (see below).



PACKAGE INFORMATION

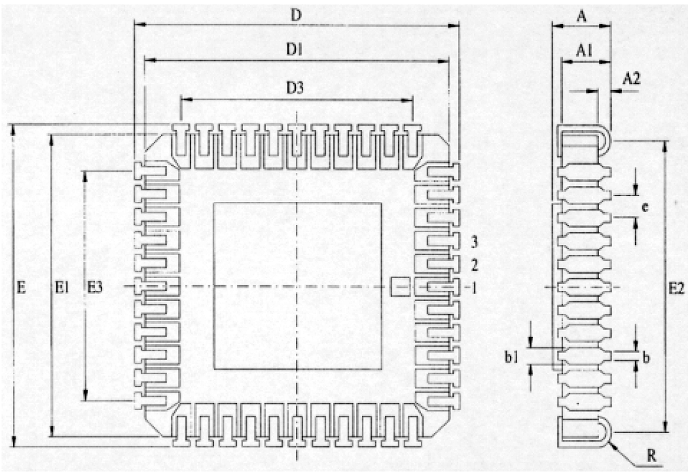


Illustration 9: Ceramic Leaded Chip Carrier, J-shaped CLDCC-J 44

DIM.	D/E	D1/E1	D2/E2	D3/E3	A	A1	A2	b1	e	b	R
min	17,15	15,75			2.92	2.16	0.51	0.56		0.33	0.51
			16,00	12,70					1.27		
max	17,78	16,76			4.83			0.89		0.58	1.02

Table 13: to Illustration 9, Dimension: mm